We claim:

1. A method for fabricating a device on a substrate, comprising:

forming a gate over said substrate;

forming a source/drain extension region in said substrate on each side of said gate, said source/drain extension regions including dopants of a first conductivity type;

forming at least one corner diffusion region in said substrate, said corner diffusion region including dopants of a second conductivity type that is opposite to said first conductivity type and overlapping with at least a portion of one of said source/drain extension regions; and

forming source and drain diffusion regions in said substrate adjacent said source/drain extension regions on opposite sides of said gate, said source and drain diffusion regions being further away from said gate than said source/drain extension regions and including dopants of said first conductivity type.

2. The method of claim 1 wherein said source/drain extension regions extend between two opposite sides of said device and said corner diffusion region overlaps with a portion of a source/drain extension region near one of said opposite sides of said device.

3. The method of claim 1 wherein said source/drain extension regions extend between two opposite sides of said device and said corner diffusion region also extends between said two opposite sides of said device.

4. The method of claim 1 wherein said device occupies an active area of said substrate, and wherein forming corner diffusion regions comprises applying a mask on said substrate that exposes at least a portion of said active area near said gate.

5. The method of claim 4 wherein said active area is bordered on some or all sides by isolation regions in said substrate, said exposed portion of said active area being near at least one of said isolation regions.

6. The method of claim 1 wherein said device is fabricated on said substrate together with a plurality of other devices and wherein said corner diffusion regions are formed during a sequence of processes for forming source/drain extensions in some of said plurality of other devices.

7. The method of claim 1, wherein said device is a PMOSFET device, wherein said source/drain extensions are formed using a PLDD implant process, and wherein said corner diffusion regions are formed using a NLDD implant process.

8. The method of claim 1, wherein said device is a NMOSFET device, wherein said source/drain extensions are formed using a NLDD implant process, and wherein said corner diffusion regions are formed using a PLDD implant process.

9. A device built on a substrate, comprising:

a gate over said substrate;

a source diffusion region and a drain diffusion region in said substrate on opposite sides of said gate;

a first source/drain extension region in said substrate between said gate and said source diffusion region;

a second source/drain extension region in said substrate between said gate and said drain diffusion region; and

at least one corner diffusion region in said substrate; said corner diffusion region overlapping with at least a portion of said second source/drain extension region; and

wherein said second source/drain extension region includes dopants of a first conductivity type and said corner diffusion region includes dopants of a second conductivity type that is opposite to said first conductivity type.

10. The device of claim 9 wherein said first and second source/drain extension regions extend between two opposite sides of said device and said corner diffusion region overlaps with a portion of said second source/drain extension region near one of said two opposite sides of said device.

11. The device of claim 9 wherein said first and second source/drain extension regions extend between two opposite sides of said device and said corner diffusion region also extends between said two opposite sides of said device.

12. The device of claim 9 wherein said device occupies an active area of said substrate, said active area being bordered on some or all sides by isolation regions in said substrate, and wherein said corner diffusion region occupies an edge portion of said active

area adjacent one of said isolation regions.

13. The device of claim 12 wherein said corner diffusion region extends under said gate.

14. The device of claim 9, wherein said device is among a plurality of devices in an integrated circuit and wherein said corner diffusion region is formed together with source/drain extension regions in some of said plurality of devices.

15. A device built on a substrate, comprising:

a gate over said substrate;

a first diffusion region and a second diffusion region in said substrate on opposite sides of said gate;

a third diffusion region in said substrate between said gate and said first diffusion region; and

a fourth diffusion region in said substrate between said gate and said second diffusion region, at least a portion of said fourth diffusion region being doped with dopants of a first conductivity type and with dopants of a second conductivity type, said first conductivity type being opposite to said second conductivity type.

16. The device of claim 15 wherein said fourth diffusion region extends between two opposite sides of said device and comprises an edge part near one of said two opposite sides and a middle part separated from said one of said two opposite sides by said edge part, said middle part being doped with only dopants of said first conductivity type and said edge part being doped with dopants of said first conductivity type and with dopants of said second conductivity type.

17. A method for fabricating an integrated circuit including NMOSFET and PMOSFET devices, comprising:

forming N-type diffusion regions in said NMOSFET devices; and

forming in at least some of said NMOSFET devices P-type diffusion regions simultaneously with at least one P-type diffusion region in at least one of said PMOSFET devices.

18. The method of claim 17 wherein said P-type diffusion regions in at least

some of said NMOSFET devices and said at least one P-type diffusion region in at least one of said PMOSFET devices is formed using a PLDD implant process.

19. The method of claim 17, further comprising forming in at least some of said PMOSFET devices N-type diffusion regions simultaneously with at least one N-type diffusion region in at least one of said NMOSFET devices.

20. The method of claim 17 wherein said N-type diffusion regions in at least some of said PMOSFET devices and said at least one N-type diffusion region in at least one of said NMOSFET devices is formed using a NLDD implant process.

21. An integrated circuit, comprising:

a plurality of NMOSFET devices, each NMOSFET device having a gate and N-type diffusion regions on opposite sides of said gate;

a plurality of PMOSFET devices, each PMOSFET devices having a gate and P-type diffusion regions on opposite sides of said gate;

wherein at least one of said NMOSFET devices includes at least one P-type diffusion region that is formed together with at least one of said P-type diffusion regions in said PMOSFET devices.

22. The integrated circuit of claim 21 wherein at least one of said PMOSFET devices includes at least one N-type diffusion region that is formed together with at least one of said N-type diffusion regions in said NMOSFET devices.